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APPLICATION NO.		FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,761		12/27/2001	Keizo Takechi	16869N-039000US	5771
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TWO EMBA	ID ANL	O TOWNSEND AN ERO CENTER	EXAMINER		
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	,	2007		ART UNIT	PAPER NUMBER
				2829	

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	licant(s)
, O#:		10/032,761	TAKECHI ET AL.
Office Action S	Summary	xaminer	Art Unit
		limmy Nguyen	2829
The MAILING DATE of Period for Reply	of this communication appea	rs on the cover shee	t with the correspondence address
A SHORTENED STATUTO THE MAILING DATE OF TH  - Extensions of time may be available after SIX (6) MONTHS from the mail  - If the period for reply specified above  - If NO period for reply is specified above  - Failure to reply within the set or exter  - Any reply received by the Office later earned patent term adjustment. See  Status	under the provisions of 37 CFR 1.136(a ing date of this communication. a is less than thirty (30) days, a reply will over, the maximum statutory period will anded period for reply will, by statute, can than three months after the mailing date.	a). In no event, however, ma thin the statutory minimum o apply and will expire SIX (6)	y a reply be timely filed  f thirty (30) days will be considered timely.  MONTHS from the mailing date of this communication.
	nunication(s) filed on <u>27 Dec</u>	cembor 2001	
2a) ☐ This action is <b>FINAL</b> .		action is non-final.	
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olosed ili accoldance	e with the practice under $Ex$	e except for formal i <i>parte Quayle</i> , 1935	matters, prosecution as to the merits is C.D. 11, 453 O.G. 213.
Disposition of Claims			
4)⊠ Claim(s) <u>1-15</u> is/are p			
	(s) is/are withdrawn	from consideration.	
5) Claim(s) is/are			
6)⊠ Claim(s) <u>1-15</u> is/are re			
7) Claim(s) is/are			
8) Claim(s) are su Application Papers	bject to restriction and/or el	ection requirement.	
9)☐ The specification is obje	ected to by the Evaminer		
10) ☐ The drawing(s) filed on		or b) abjected to b	utho Eveninas
	est that any objection to the dra		
11)☐ The proposed drawing o	correction filed on is:	a) approved b)	disapproved by the Exeminer
	rawings are required in reply to		a disapproved by the Examiner.
12) The oath or declaration			
Priority under 35 U.S.C. §§ 119			
13) Acknowledgment is ma	ade of a claim for foreign pri	ority under 35 U.S.C	: 8 119(a)-(d) or (f)
a)⊠ All b)⊡ Some * c)[		,	. 3 113(a)-(a) of (i).
	— of the priority documents ha	ve been received	
	of the priority documents ha		Application No
<u> </u>			n received in this National Stage
application tr	om the International Bureau d Office action for a list of th	⊦(PCT Rule 17 2(a\)	
14) ☐ Acknowledgment is made	e of a claim for domestic pri	ority under 35 U.S.C	C. § 119(e) (to a provisional application).
a) ☐ The translation of the standard of the s	he foreign language provisio	nal application has	been received
Attachment(s)	·		
1) Notice of References Cited (PTO-8 2) Notice of Draftsperson's Patent Dra 3) Information Disclosure Statement(s	wing Review (PTO-948)	4) Interview 5) Notice o 6) Other:	v Summary (PTO-413) Paper No(s) f Informal Patent Application (PTO-152)
Patent and Trademark Office O-326 (Rev. 04-01)	Office Action S	Summary	Part of Paper No. 4

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#### **DETAILED ACTION**

#### Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 1 5, 10, 11, 13, 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Person (US 5521493).

#### As to claim 1, Persons discloses (fig 4)

A driver circuit integrated with a load current output circuit (401), wherein driver circuit integrated with a load current output circuit (401) has a function as driver for applying a predetermined test waveform to a DUT (101), and a function as a load current output for reproducing an actual use situation by receiving load current to DUT (101) to judge a response (by the comparator 403) waveform by receiving response waveform from DUT (101), both functions being made up on a common circuit, operates as driver circuit when applying test waveform, and operates as load current output circuit when judging response waveform (as seen in the figure 4).

# As to claim 2, Persons discloses (fig 4)

A driver circuit integrated with a load current output circuit (401), comprising: a buffer circuit (409) for a push pull operation, a constant current

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portion (VIH, VIL, VCOMM), a current control portion (420) connected to an output terminal of buffer circuit (409) and constant current portion and constituted of an one way conduction element capable of supplying a current of one direction or reversed direction with respect to DUT (101), wherein driver function and load current output function are provided by controlling current at constant current portion.

### As to claim 3, Persons discloses (fig 4)

A driver circuit integrated with a load current output circuit (401) wherein current control portion (407) comprises a first terminal connected to buffer circuit (409), a second terminal connected to constant current portion (401a), and a third terminal for supplying a current to DUT (101).

# As to claim 4, Persons discloses (fig 4)

A driver circuit integrated with a load current output circuit (401) wherein buffer circuit (409) is provided with switches (SW2) for controlling the push pull operation of buffer circuit.

# As to claim 5, Persons discloses (fig 4)

A driver circuit integrated with a load current output circuit wherein current control portion is a diode bridge circuit (407).

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As to claims 10 and 11, 13, 14, Persons discloses (fig 4) a pin electronic (400) IC provided with driver circuit integrated with load current output circuit.

#### Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

4. Claims 6 – 9, 12, 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Takeuchi (US 4523312).

As to claims 6, 7, Takeuchi discloses (fig 5)

A driver circuit integrated with a load current output circuit (1) comprising: a first buffer circuit (39i) having a first output terminal; a second buffer circuit (41i) having a second output terminal; and a diode bridge terminal (6i) having a pair of a third and fourth output terminals each connected to first (3i) and second output terminals (41i), wherein fourth output terminal (connect to 5i) supplies a current as a driver when outputting a test waveform to a DUT (10), and DUT (10) supplies a load current to fourth output terminal therefrom by turning the second buffer (41i) circuit OFF when judging a status of a response waveform by receiving waveform from DUT (10).

<sup>(</sup>b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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As to claims 8 and 9, 12, 15, These limitations are inherently within the scope of invention.

#### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner-should be directed to Jimmy Nguyen at (703) 306-5858. Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4900.

JN. April 3, 2003

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SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2800